Powering Noise Sensitive Loads

Analog Devices August 2013

ARROW
Five Years Out

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Agenda

- **Understanding Load Requirements (generic guidelines)**

- **Getting the most out of the LDOs**

- **Low noise design with switching regulators**

- **Intro to ADIsimPower**

Everyone needs power
many application require low noise designs

Sensors

Amp

ADC

RF

Clock

Isolation

Reference

Power
Analog_POL
Noise/PSRR
SW vs. LDO

Processors

FPGAs

Power
Digital_POL
High Current, Switcher
Vin, Vout, Load current, Vaccuracy, Sequencing

DAC

Clock

Isolation

Reference

Amp

RF

Power
Analog_POL
Noise/PSRR
SW vs. LDO

Power
System
distribution

ADIsimPower
VOLTAGE
REGULATOR
DESIGN TOOL

ADI Products

Partner Products

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Identify noise sensitive loads

◆ **When it comes to powering analog loads the requirements published by semiconductor manufacturers are traditionally been very vague**

◆ **Analog IC suppliers specify performances with ideal power supplies and suggest only the use of only LDO to power ADCs, DACs, Amps, etc.**
- **Some IC datasheets specify PSRR but often only at DC or 1Khz**

◆ **ADI is changing its practices to show more of a system level approach to powering solutions**
- **Not just at the IC level but at the system level**

◆ **Where can I find information on ADI's parts?**
  - ◆ Datasheets
  - ◆ Eval boards documentations
  - ◆ CFTL (Circuits from the lab web site) - www.analog.com./CFTL
  - ◆ ADI Wiki pages - http://wiki.analog.com/
  - ◆ Growing list of reference designs

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Common Characteristics of Analog loads

◆ **Almost all analog loads have decent PSRR at low frequency**
  - **Users need to understand what frequency ranges matter to the application and analyze power supply noise over frequency**
  - **PSRR is typically good to 1/10 of IC bandwidth for Amplifiers**
    - Example 1: a ADA4932 1Ghz Differential amplifier has >60dB PSRR up to 100Mhz
   - Example 2: ADA4898 60Mhz op-amp has <40dB at 6Mhz
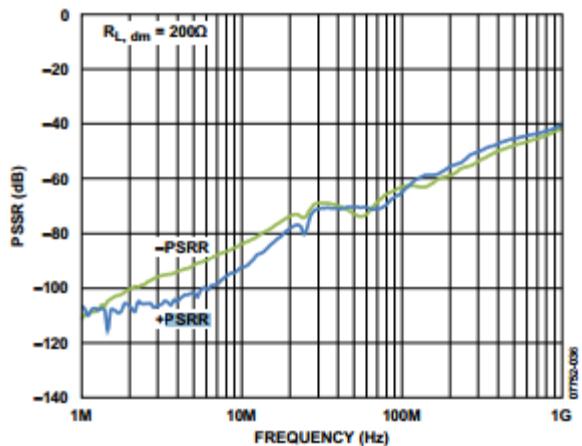
Figure 36. PSRR vs. Frequency
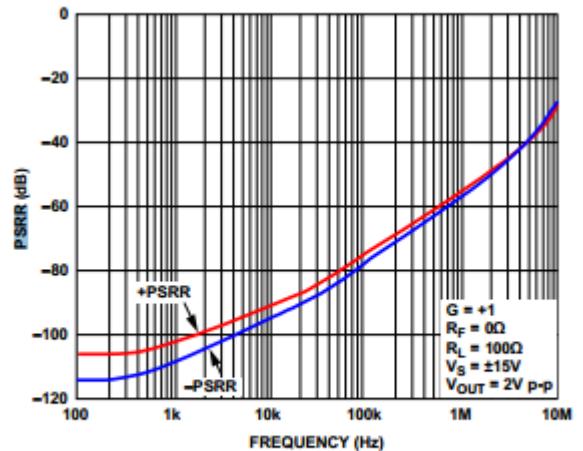
Figure 33. Power Supply Rejection Ratio (PSRR) vs. Frequency

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Translating PSRR to noise requirement

◆ **Most devices can tolerate some level of power supply noise**
  - **But high performance products means low noise designs**

◆ **Example 16bit 125Msps ADC**
  - **SFDR = 100dBFS**
  - **Equivalent to 10uV spur levels**

AD9268 DUT_AVDD Signal level to bring spur to noise floor
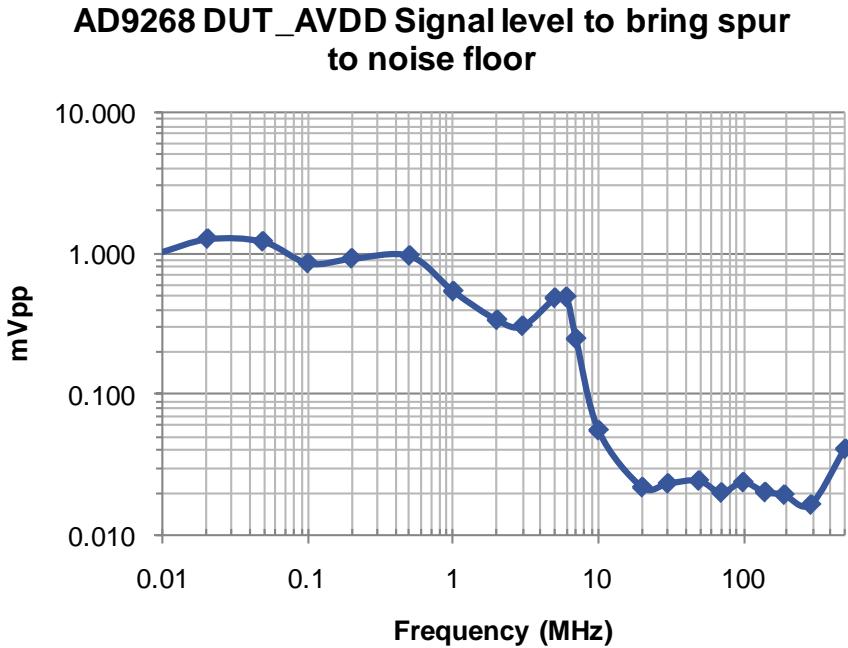
◆ **Required power supply noise <800uV from 100khz – 1Mhz**
◆ **<20uV above 10Mhz**
  - **Achievable with LDOs after adequate switcher filtering**
  - **Spurs control done with layout and appropriate filtering**

Common Characteristics – cont.

- **Most low-noise/analog apps behave like a DC loads to the power supply; no transient load**
  - **Exception are RF PA in burst mode TX mode (TDMA radio)**

- **Let's look at the sensitivity for common low-noise apps**
  - **LS - Low-Sensitivity tolerates 10s of mV (up to 100mV of ripple)**

  - **MS - Low-Sensitivity tolerates mV (20mV of ripple)**

  - **HS - Medium sensitivity, tolerates 100's of uV**

  - **VHS - Very High sensitivity, needs < 100uVrms**
  - **Very demanding requirements needing a lot of filtering and attention to layout, crosstalk and noise spectrum (not just ripple)**

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Digital Loads Requirements guidelines

	Low end FPGA	High End FPGA	DSP/uC	Memory
% of digital Content	100%	80%	90%	90%
Unique Power requirements	No	Sequencing, PLL power	DDR Termination	Sequencing, PLL power
Target specs (DC Accuracy)	5%	5%	5%	1-2%
Voltage Transient	5%	3%	3%	2%
Noise sensitivity	No	No	No	Med
Ripple	100mV (3%)	50mV (2%)	50mV (2%)	20mV-50mV (1-2%)
Typical Power Solution	Switcher	Switcher	Switcher	Switcher

Noise Sensitivity scale			
Low	med	high	Very High
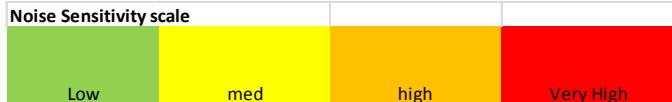
Analog Loads Requirements guidelines

	Amps	Mixers/RF	RF PA
% of Analog	99%	99%	100%
Analog Section	Amps	Amps	Bias gain control, Amp
Digital section	Gain control	Gain Control	-
Unique Power requirements	Low noise design/Layout	Low noise design/Layout	Low 1/f noise and high transient
Target specs (DC Accuracy)	5%	5%	5%
Transient	load dependent	not critical	Operation dependent (TDM)
Noise Sensitivity	high > 10Khz	high DC to Ghz	Very high DC to Ghz
Ripple/noise	100uV	100uV	10uV
Typical Power Solution	Switcher + LDO or Filtered switcher	Switcher + LDO or Filtered switcher	Low noise high speed LDO with headroom

Noise Sensitivity scale			
Low	med	high	Very High
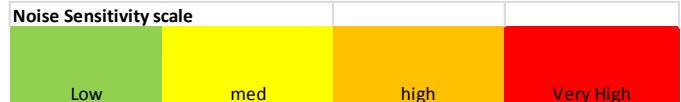
Mixed Signal Loads Requirements guidelines

	ADCs	DACs	PLL/VCO/Clock Gen	Trasceivers (radio on a chip)
% of Analog	50%	50%	50%	80%
Analog Section	S/H, Amps, Clocks	S/H, Amps, Clocks	VCO PDF Charge Pump	ADC/DAC/RF/VCO/PA
Digital section	Digital core and interface	Digital core and interface	Dividers/Drivers	Digital Core and Interface
Unique Power requirements	Low noise design/Layout/Crosstalk	Low noise design/Layout/Crosstalk	Low 1/f noise, Layout Crosstalk	Low 1/f noise and high transient
Target specs (DC Accuracy)	5%	5%	5%	2%
Transient	not critical	not critical	not critical	Operation dependent (TDM)
Noise Sensitivity	High >100khz	High >100khz	Very high DC to Ghz	Very high DC to GHz
Ripple/noise	100uV – 1mV (resolution dependent)	100uV – 1mV (resolution dependent)	10uV – 100uV (Performance dependent)	10uV10uV – 100uV (Performance dependent)
Typical Power Solution	Switcher + LDO or Filtered switcher	Switcher + LDO or Filtered switcher	Very Low noise LDO with headroom	Filtered switcher + Low noise LDO and high BW LDOs
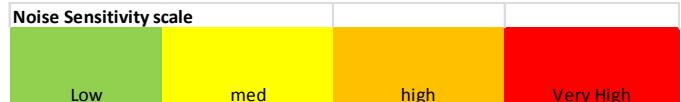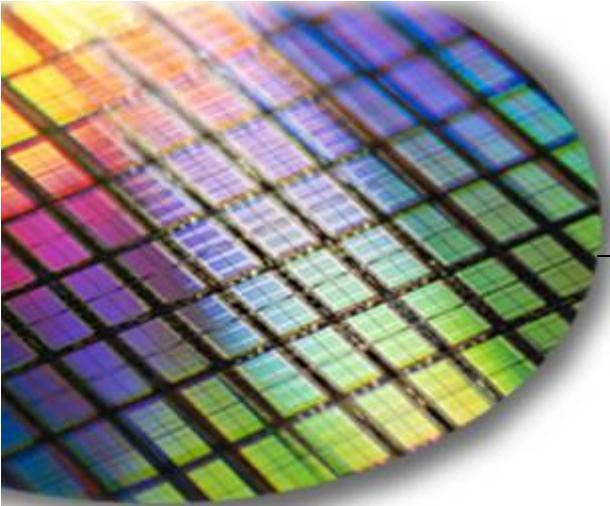
Noise Sensitivity scale			
Low	med	high	Very High

Getting the most out of the LDO

Make sure you get all the performance you paid for

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PSRR – Power Supply Rejection Ratio

◆ **A measure of how well a circuit rejects ripple at various frequencies coming from the input power supply**
- **PSRR is expressed in dB, and is plotted on a log scale of dB Vs Frequency**
- **Frequency range of interest is usually 10Hz to 10MHz**

◆ **Devices with good PSRR typically have high gain and a high unity gain frequency**
- **PSRR is often better for LDOs with higher quiescent current**

◆ **PSRR is typically specified with a healthy headroom**
- **ADI datasheet start to specify PSRR at 500mV or lower**

1.5V – 2V headroom In most datasheets

Vin
Vin Ripple
0
Tir Vout
Vout Ripple
0
Time

V_{RIPPLE} = 50mV p-p
V_{IN} = 5V
V_{OUT} = 3.3V
C_{OUT} = 2.2µF
I_{LOAD} = 100mA

PSRR (dB)
FREQUENCY (Hz)

06110-040

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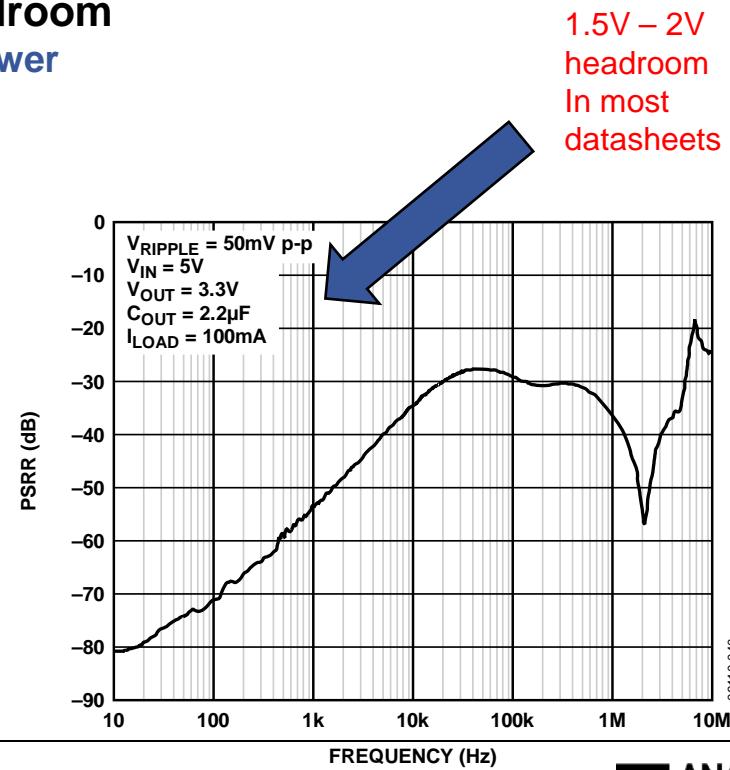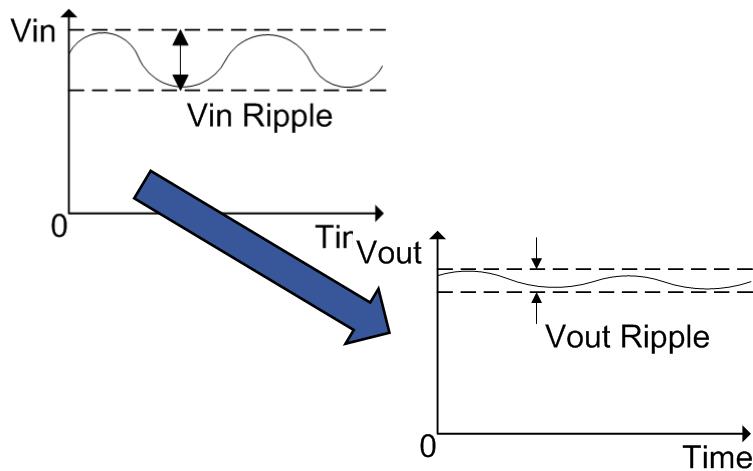
LDO PSRR is a Function of Frequency

- The relationship between the error amplifier gain bandwidth and PSRR is shown below.
- This example is a highly simplified case where the output capacitor and circuit parasitics are ignored. LDO loop gain bandwidth is assumed to be 3MHz
- Most switching regulators operate outside the roll of point
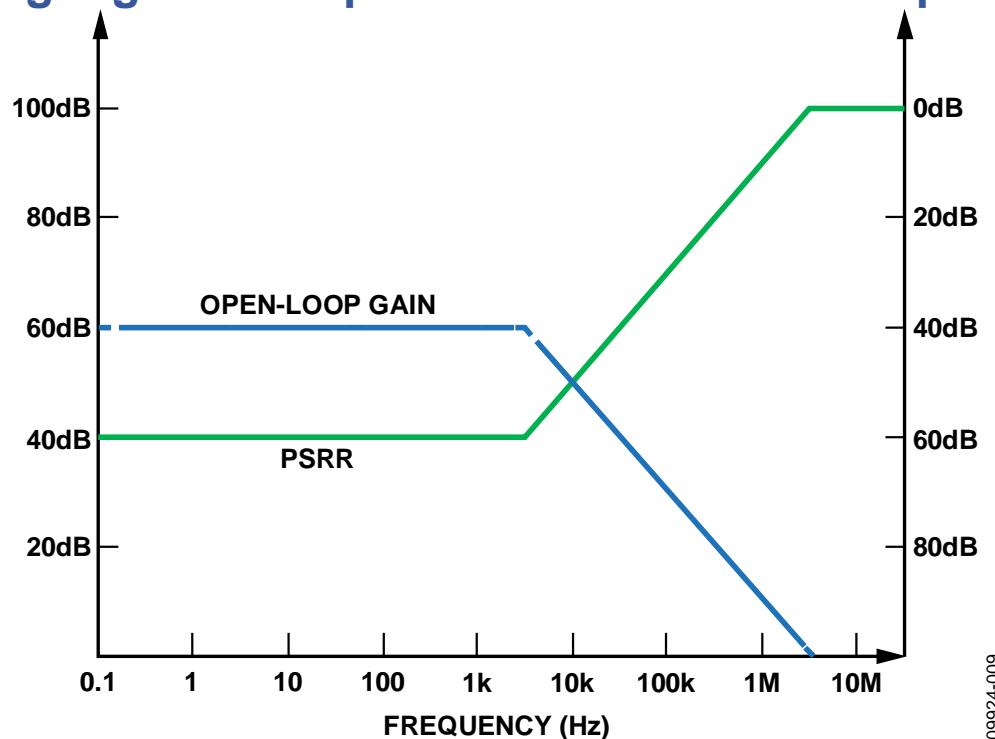
Contributors to PSRR

- **The PSRR plot below shows three main frequency domains that characterize the PSRR of an LDO**
  - **Reference PSRR region**
    - Bandwidth of the reference amplifier and internal reference filtering
  - **Open-loop gain region**
    - Function of the error amplifier gain bandwidth
  - **Output capacitor region**
    - Dominated by the cap ESR and ESL/SRF (series resonant frequency)
    - It is possible to optimize this by selecting a combination of caps (10uF + 1uF)
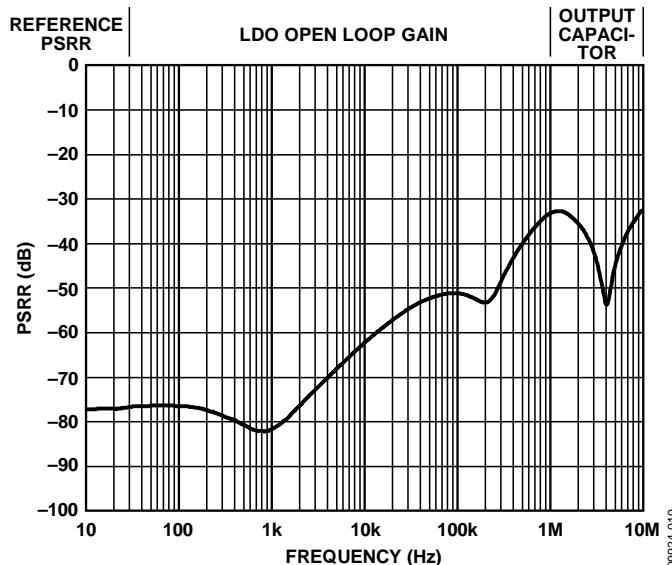
Dropout

- **Dropout is the phenomenon that occurs when the regulator input voltage approaches the nominal output voltage.**
- **Pass device transitions from the saturation region (acts like a current source) to the linear region (acts like a resistor)**
- **$V_{DROPOUT}$ = Load Current x ON-Resistance$_{(PMOS)}$**

- **Most modern regulators are low dropout regulators (LDO)**

- **But do not operate in or very near drop out!**
  - **You need headroom to maintain regulation and PSRR**

Vout Vs Vin (In Dropout)

—	100uA
—	10mA
—	100mA
—	250mA
—	360mA
—	500mA

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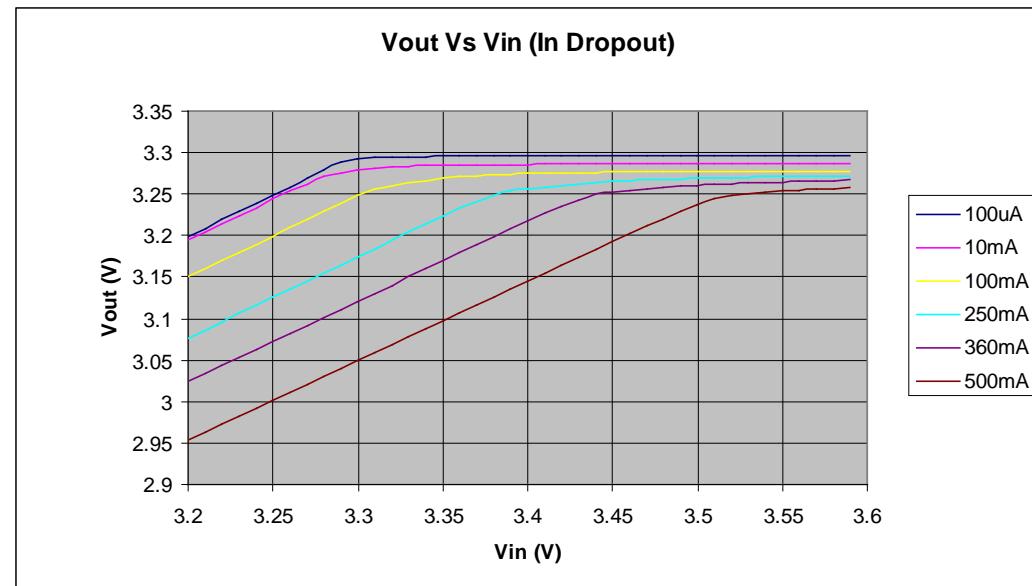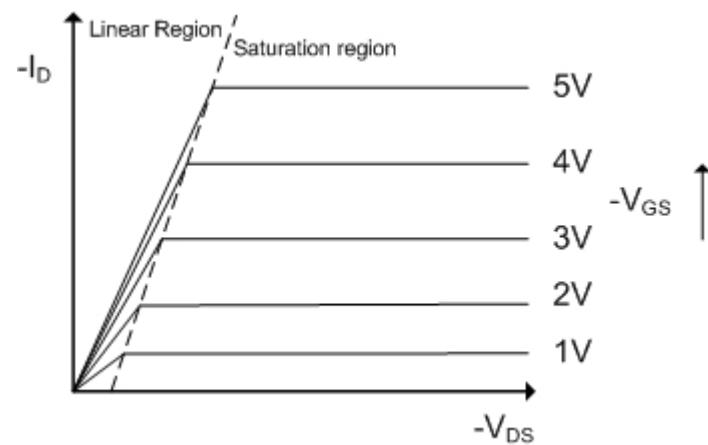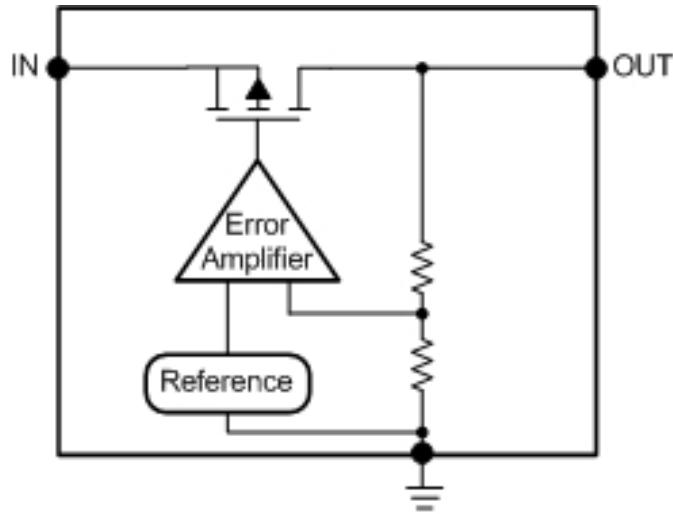
Ex: ADP7104 PSRR vs. Headroom
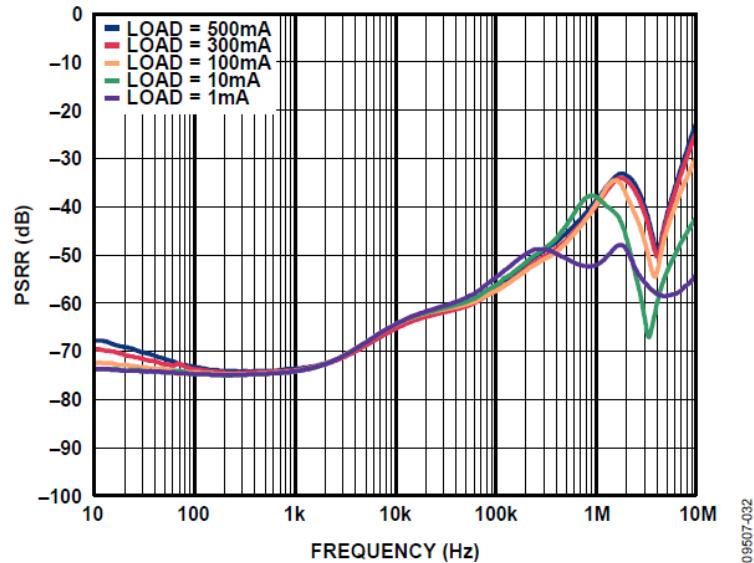
Figure 37. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 6.5 V
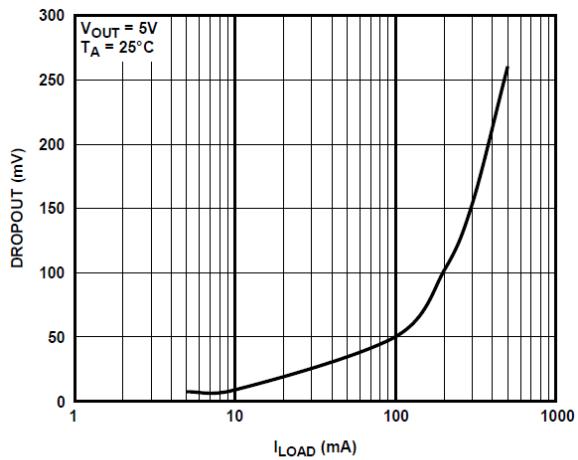
Figure 20. Dropout Voltage vs. Load Current, V_{OUT} = 5 V
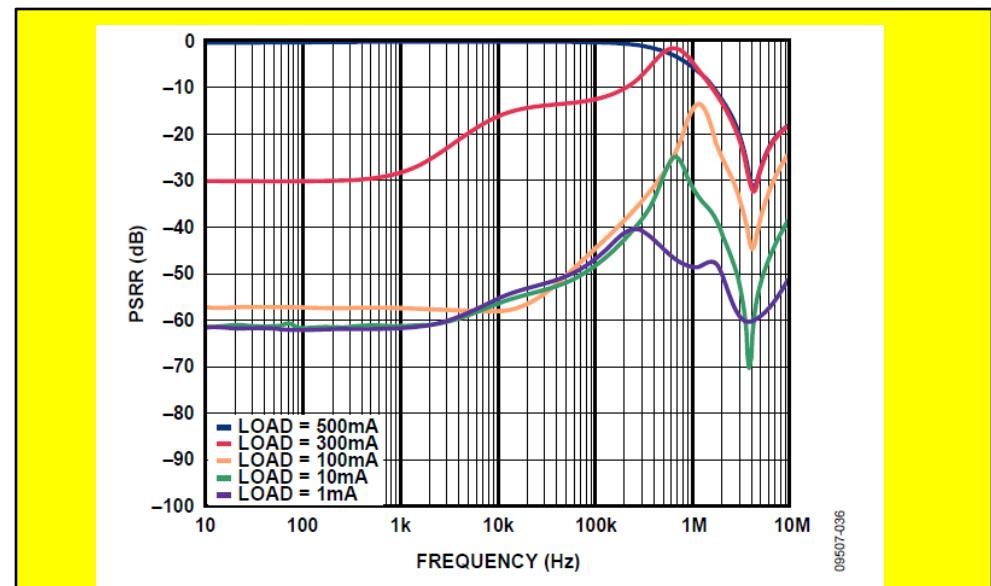

Figure 41. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, V_{IN} = 5.2 V

200mV example, 0dB PSRR at full load

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Why High PSRR and Low Headroom are Mutually Exclusive

- **The gain of the pass element decreases as it leaves saturation and enters the triode region of operation**
  - **If Vin is too close to Vout**
  - **As the load current increases gain decreases**

- **This causes the overall loop gain of the LDO to decrease, resulting in a lowering of the PSRR.**

- **The smaller the headroom is, the more dramatic the reduction in gain.**

- **At some small headroom voltages, the control loop has no gain at all, and the PSRR falls to zero**

Common Issues Applying Linear Regulators

◆ **Insufficient Headroom**
- **Temperature increases Rdson, increasing drop-out**
  - ◆ Look for the worse case guaranteed and add margin to it
- **PSRR strong function of headroom**
  - ◆ Any voltage drop across the RDSON due to the load current, subtracts from the headroom of the active portion of the pass element

◆ **LDOs are often used near drop-out to filter switching regulators ripple noise**
- **Loop gain rolls off and reduced headroom means LDO becomes "RC filter" at high frequencies**
- **Switching regulator frequency is outside the loop bandwidth**
  - ◆ At 500Khz most LDOs have <10dB PSRR when in dropout

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LDO PSRR – summary

- **LDO PSRR is a function of frequency**
  - **Loop gain bandwidth limitations**

- **LDO PSRR is a function of load current**
  - **Output impedance decreases as load increases**
    - Output pole increases in frequency

- **LDO PSRR is a function of headroom**
  - **RDS_{ON} further decrease effective V_{DS} across FET**

- **high PSRR and low headroom are mutually exclusive**
  - **FET operating point**
    - Saturation vs triode region
  - **LDOs in drop-out are not good switching regulator filters**

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Cascading LDOs for very high PSRR

- **In applications with adequate headroom, cascading LDOs can greatly improve PSRR.**
- **The figure below shows a simplified schematic of the ADM7150 LDO.**
  - The internal power supply block is essentially an LDO whose output voltage is 500mV higher than V_{OUT}.
  - This isolates the main LDO input from any noise on V_{IN}
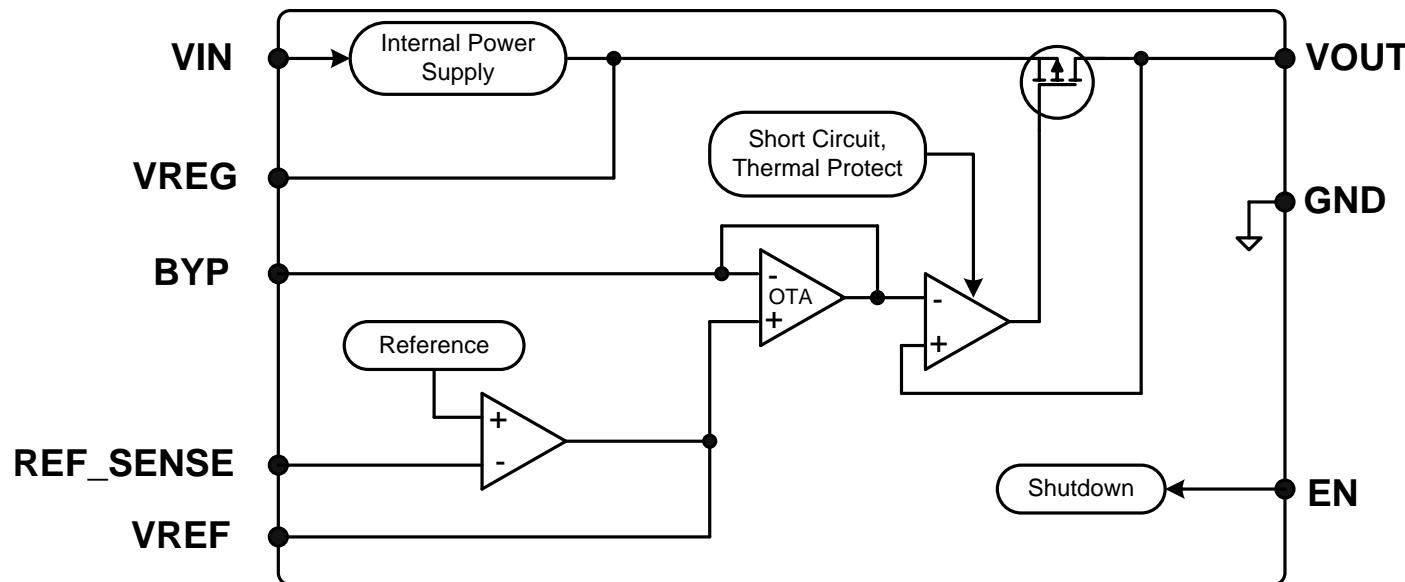
Cascading LDOs for Very High PSRR

- **Single vs Cascaded LDO PSRR at same headroom and load current**

Single vs Cascaded LDO PSRR
ADM7160 vs ADM7150
100mA/1V Headroom
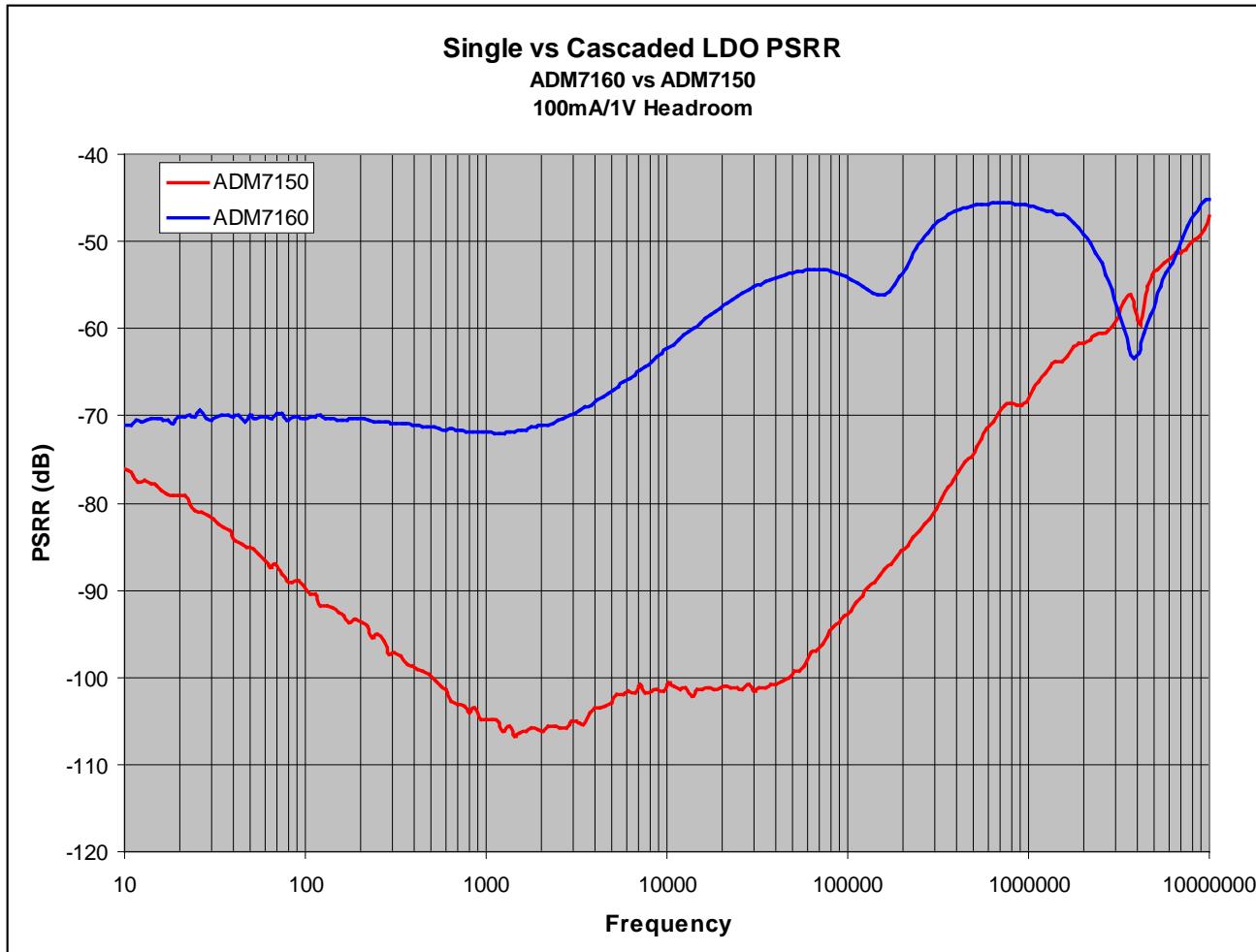
Comparing LDO PSRR Specifications

- **When comparing LDO PSRR specifications, ensure that the measurements are made under the same test conditions.**
  - Many older LDOs specify PSRR at only 120 Hz or 1 kHz with no mention of headroom voltage or load current.
  - If headroom is specified it is often set to 1V or 2V
    - Many ADI LDOs now specify performance at 200mV to 500mV headroom

- **PSRR in the electrical specification table should be listed for different frequencies.**
  - Ideally, typical characteristic plots of PSRR under different load and headroom voltages should be used to make meaningful comparisons.

- **The output capacitor also affects the LDO PSRR at high frequency.**
  - The capacitor value and type is especially important
  - at frequencies above the error amplifier 0 dB crossover frequency, where the attenuation of power supply noise is a function of the output capacitance.

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Sources of Noise in LDOs

◆ **Simplified block diagram of an LDO circuit showing intrinsic and extrinsic noise sources**
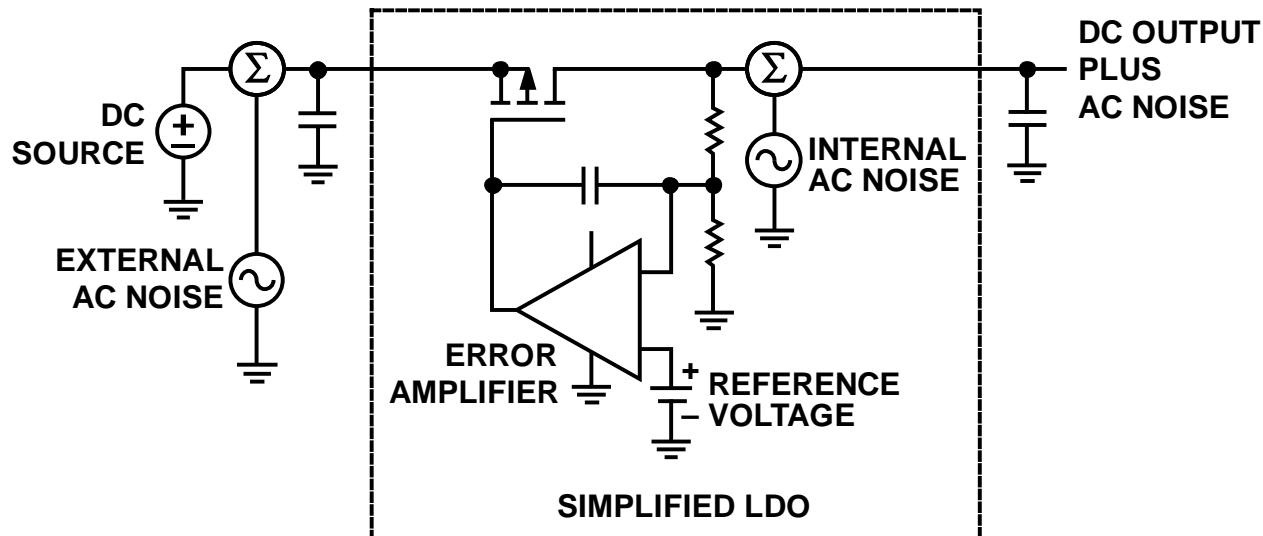
Feedback resistors: noise defined as Vn = √(4kTRB)

LDO Noise Reduction Techniques

◆ **There are two major methods for reducing the noise of an LDO:**
- ● Filtering the reference
- ● Reducing the noise gain of the error amplifier

◆ **LDOs with external capacitor to filter the reference**
- ● Many so-called ultralow noise LDOs require the use of an external noise reduction capacitor to achieve their low noise specifications. The drawback of using external filtering of the reference is that the start-up time is proportional to the size of the filter capacitor

◆ **Reducing the noise gain of the error amplifier does not have as dramatic an effect on the start-up time as filtering the reference, thus making the trade-off between start-up time and output noise easier**
- ● Unfortunately, reducing the output noise is generally not possible for fixed output LDOs because there is no access to the feedback node. However, the feedback node is readily accessible in most adjustable output LDOs

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LDO Noise Reduction Techniques

- Reducing the AC noise gain
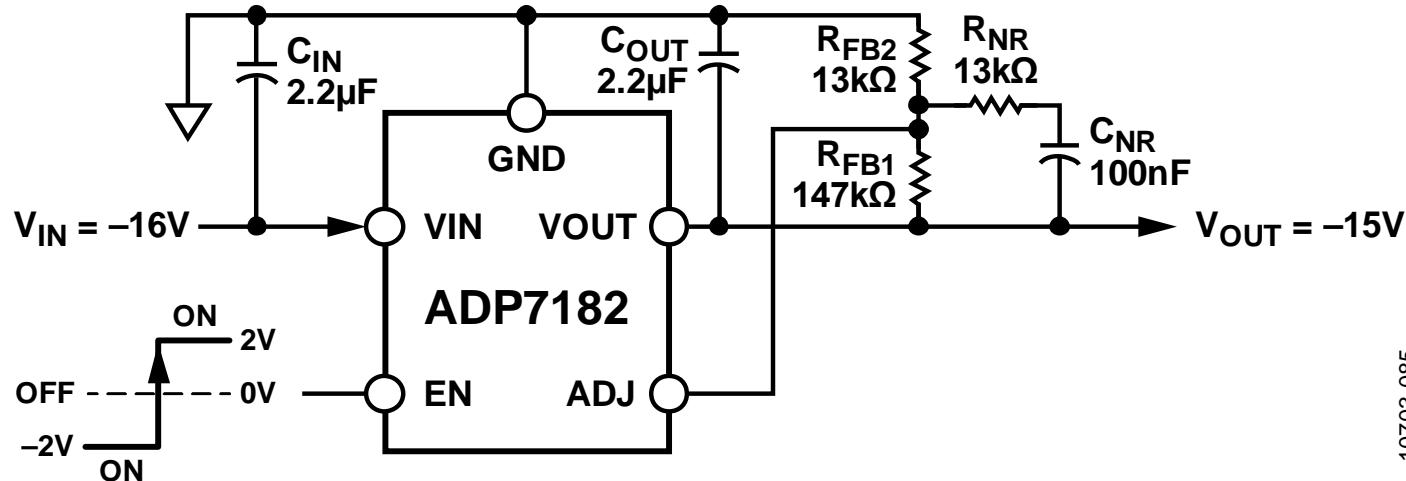
- **The noise of the LDO is approximately the noise of the fixed output LDO (typically 18 μV rms) times the high frequency ac gain. The following equation shows the calculation with the values shown**

$$18\,\mu V \times \left(1 + \left(\frac{1}{1/13\,\mathrm{k\Omega} + 1/147\,\mathrm{k\Omega}} \right) / 13\,\mathrm{k\Omega} \right)$$

LDO Noise Reduction Techniques
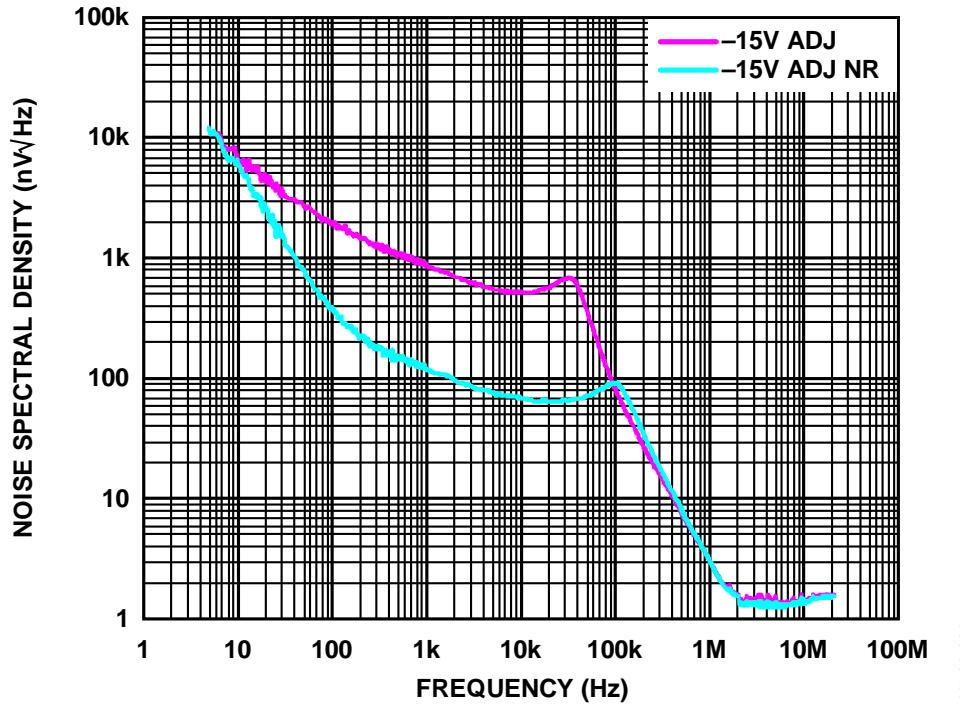
- **The figure above shows the difference in noise spectral density for the adjustable ADP7182 set to −15V with and without the noise reduction network.**
- **In the 100 Hz to 30 kHz frequency range, the reduction in noise is almost 20dB.**

LDO Noise Reduction Techniques
- Filtering the Reference

◆ **ADM7150 – Noise Reduction**
- **A capacitor (C_{BYP}) is connected to BYP to filter the error amplifier reference voltage**
- **Increasing C_{BYP} will reduce the LDO noise, improve PSRR and increase start up time**
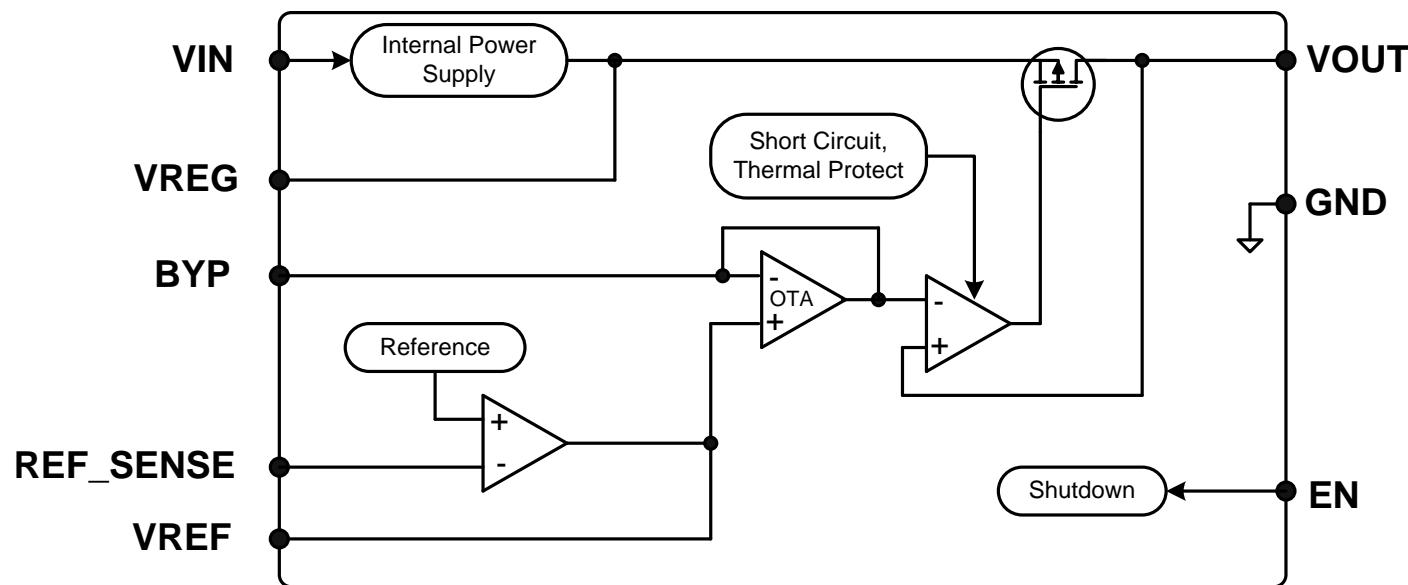
LDO Noise Reduction Techniques

- **ADM7150 – NSD vs C_{BYP}**

ADM7150 NSD vs Frequency Different C_{BYP}
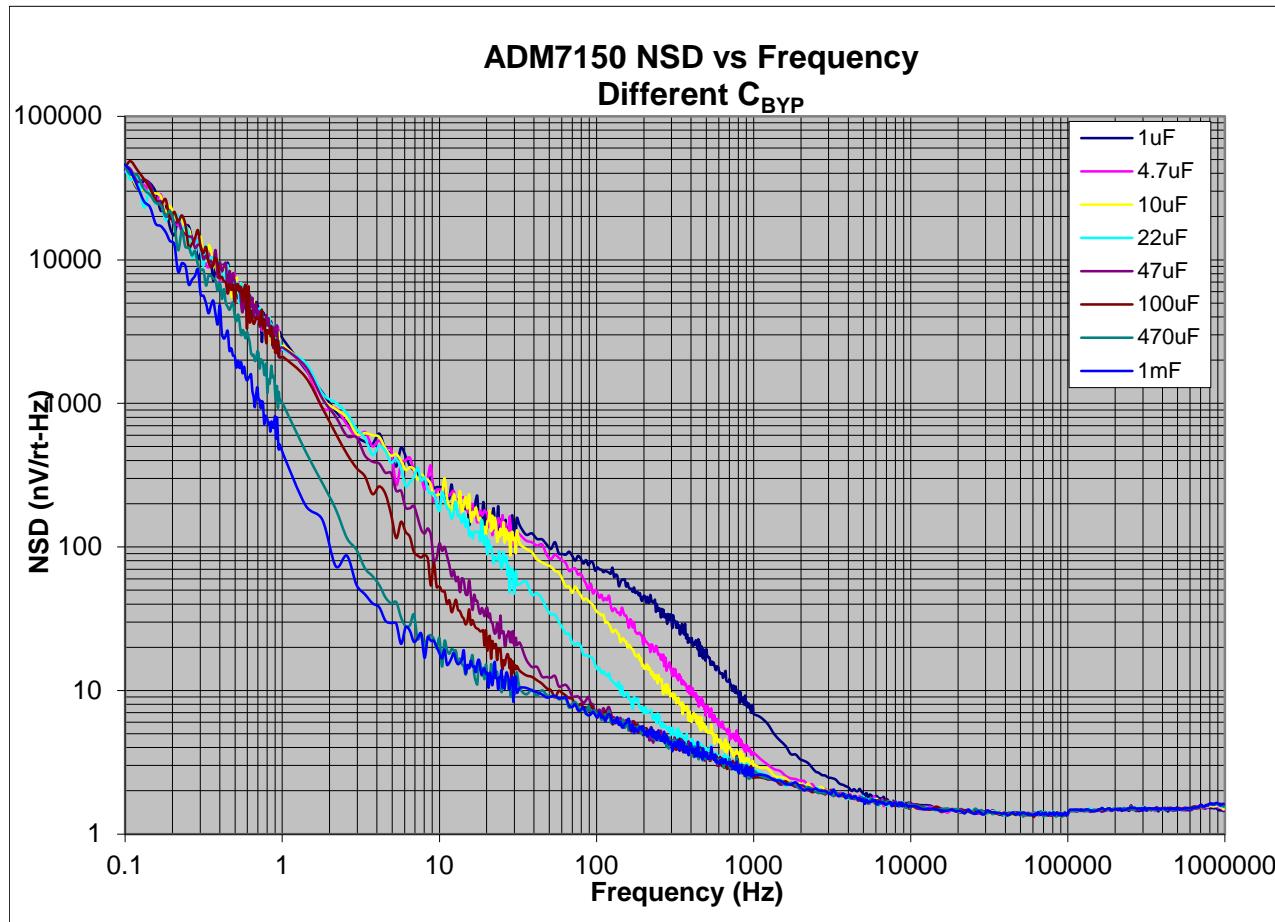
Comparing LDO Noise Specifications

- ◆ **Comparing LDO Noise Specifications**
  - ● **When comparing LDO noise specifications, ensure that the measurements are made under the same test conditions**
    - ◆ Vout set point is very important
    - ◆ In many LDOs noise is directly proportional to Vout

  - ● **RMS noise (Vrms) – noise integrated over a specified bandwidth**
    - ◆ Many LDOs specify rms noise over a bandwidth of 100Hz to 100KHz. This makes the noise look lower than noise measured over 10Hz to 100kHz, especially if the LDO has high 1/f noise

  - ● **Noise Spectral Density (NSD) – noise at frequency in nV/Sqrt(Hz)**
    - ◆ At the least, NSD in the electrical specification table should be listed for several different frequencies.

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What does a good LDO buy you?
Example PLL Phase Noise (at 4.4GHz) vs. Frequency Offset
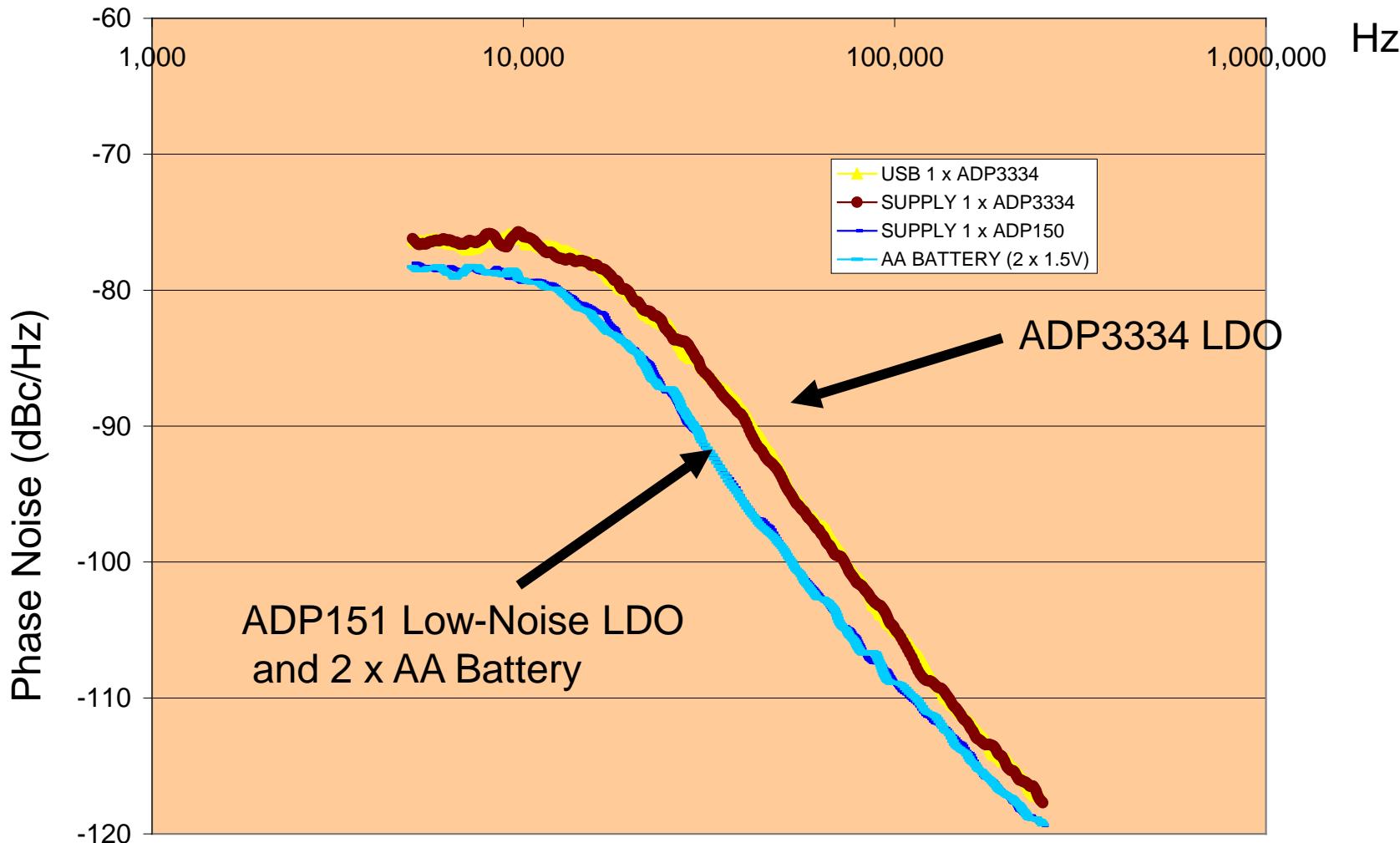
Example of some New LDOs from ADI Performance advantages

- **ADM7160 – Low power ADC/DAC circuits**
  - ◆ Fixed outputs
  - ◆ Load noise (10uVrms) and good PSRR (54dB at 100Khz)

- **ADP7182 – Opamp Circuits Negative Supply**
  - ◆ Fixed and adjustable
  - ◆ Input voltage range -2.7 to -28V
  - ◆ Low noise (15uVrms) and good PSRR (66dB at 100Khz)

- **ADM7150 – RF/VCO/PLL circuits**
  - ◆ Best in class noise
    - <1.5nV/rt-Hz @ 10KHz, <2uVrms @ 10Hz to 100KHz
  - ◆ Very high PSRR
    - >90 dB from 500Hz to 100KHz @ 400mA, 1.2V headroom

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Resources

◆ **AN-1120: Noise Sources in Low Dropout (LDO) Regulator**

◆ **AN-1099: Capacitor Selection Guidelines for ADI LDOs**

◆ **ADM7150 datasheet**

◆ **ADM7160 data sheet**

◆ **ADP7182 datasheet**

◆ **ADP7102 & ADP7104 datasheets**

◆ **AN-1106: An improved dual supply architecture (SEPIC-CUK)**
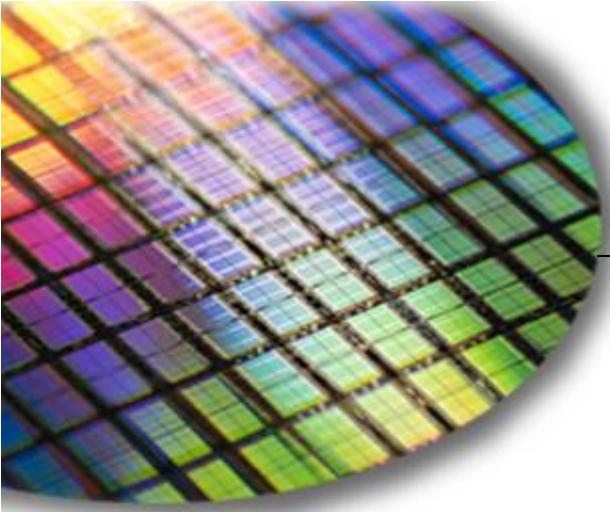
Powering the LDO
or the next link in the system level power design

System level tradeoffs
Headroom and/or filtering

- ◆ **If system can afford space/power loss, use a switcher to run an LDO**
  - ● **LDO performance degraded with low headroom**

5.0V @ 0.26A ──── **DC/DC (90% eff)** ──── **2.3V @ 0.5A** **LDO** ──── **1.8V @ 0.5A** **ADC**
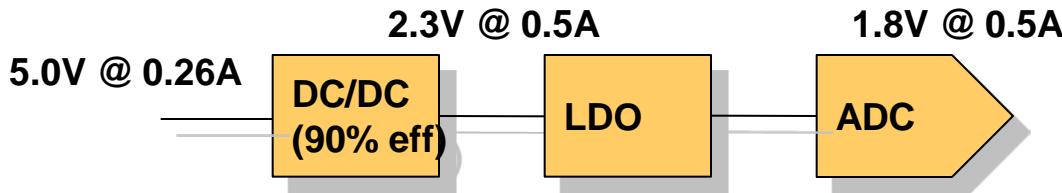
Power Lost: 0.13W+0.25W = 0.38W

- ◆ **Using only an LDO:**
  - ● **Best performance achievable**
  - ● **At the cost of heat**

5.0V @ 0.5A ──── **LDO** ──── **1.8V @ 0.5A** **ADC**
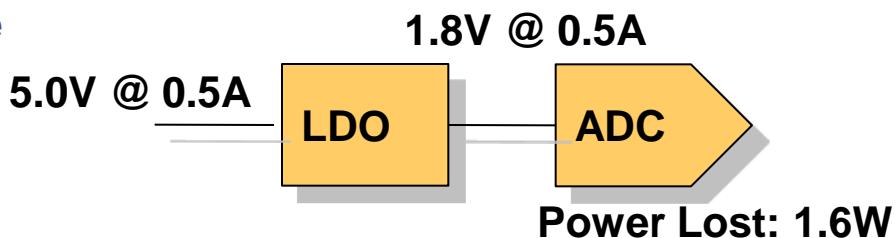
Power Lost: 1.6W

- ◆ **Using a Low-Noise Switcher:**
  - ● **very noise sensitive systems such as PLLs cannot afford this**

5.0V @ 0.21A ──── **DC/DC (85%eff)** ──── **1.8V @ 0.5A** **ADC**

Power Lost: 0.16W

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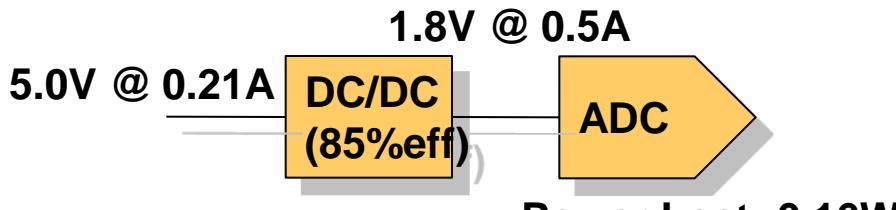
Are Switching regulators noisy?

- **It depends – with adequate design the noise can be managed**
  - Ripple level is managed with switching frequency and output capacitance selection
- **Careful layout is very important**
  - Input capacitor and power ground
- **Switching frequency is a know frequency**
  - It is not "noise", but rather a coherent and predictable signal
  - Can also be synchronized
- **Relatively easy to filter**
  - LC filters and ferrite beads recommended
- **Current mode controllers noisier than voltage mode**
  - With careful layout the can be made quiet

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How to do Power Layout in 2 Slides

Red is the most important, least obvious loop.

Blue and green loops should be same size

Cin — Need well placed low ESR, low ESL ceramic input capacitors

Need well placed ceramic output capacitors

Better Layout
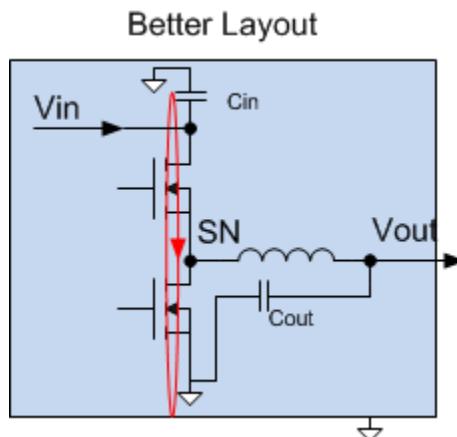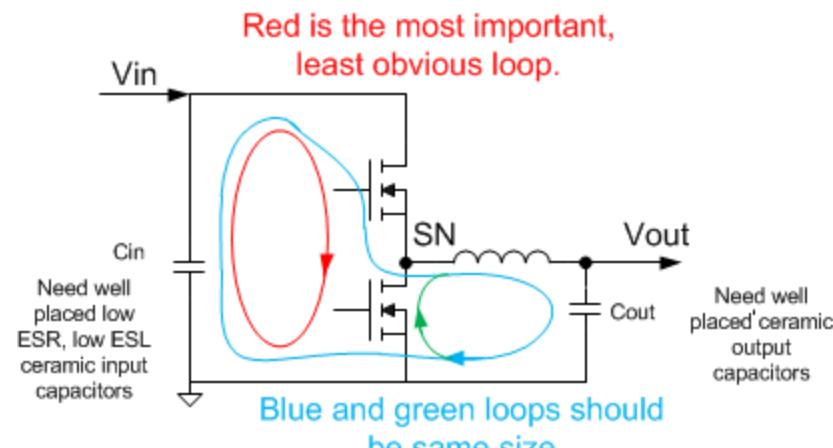
- ◆ **Current flows in Loops**
- ◆ **Lowest inductance, layout has current return path under current path**

- ◆ **Every inch on every layer should be ground plane**
  - • **Reduces parasitic inductance**
  - • **Shorts out EMI noise**
  - • **Helps thermal dissipation**
- ◆ **Never autoroute power traces**
- ◆ **Use plenty of vias (0.5 A each depending on size)**
  - • **Also helps with thermals**
  - • **Can reduce parasitic inductance**
- ◆ **Size trace thickness according to current to carry**
  - • **All main power traces should be polygon fills**

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Importance of the input capacitor


CIN ESL = 0.3nH (Typ. for 0402)
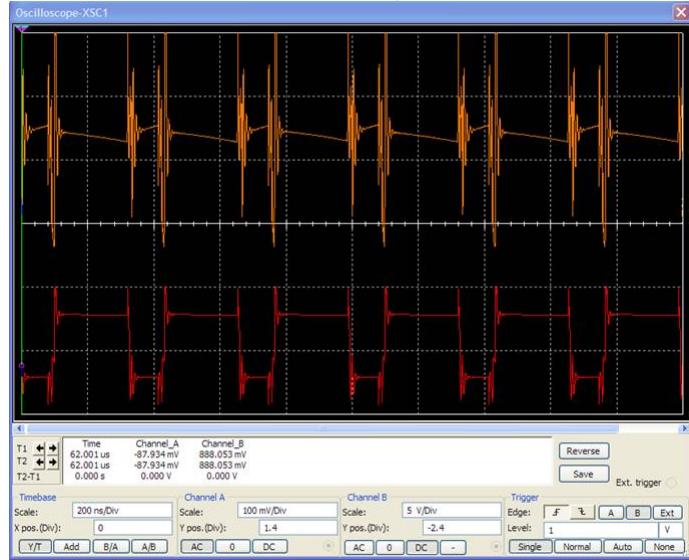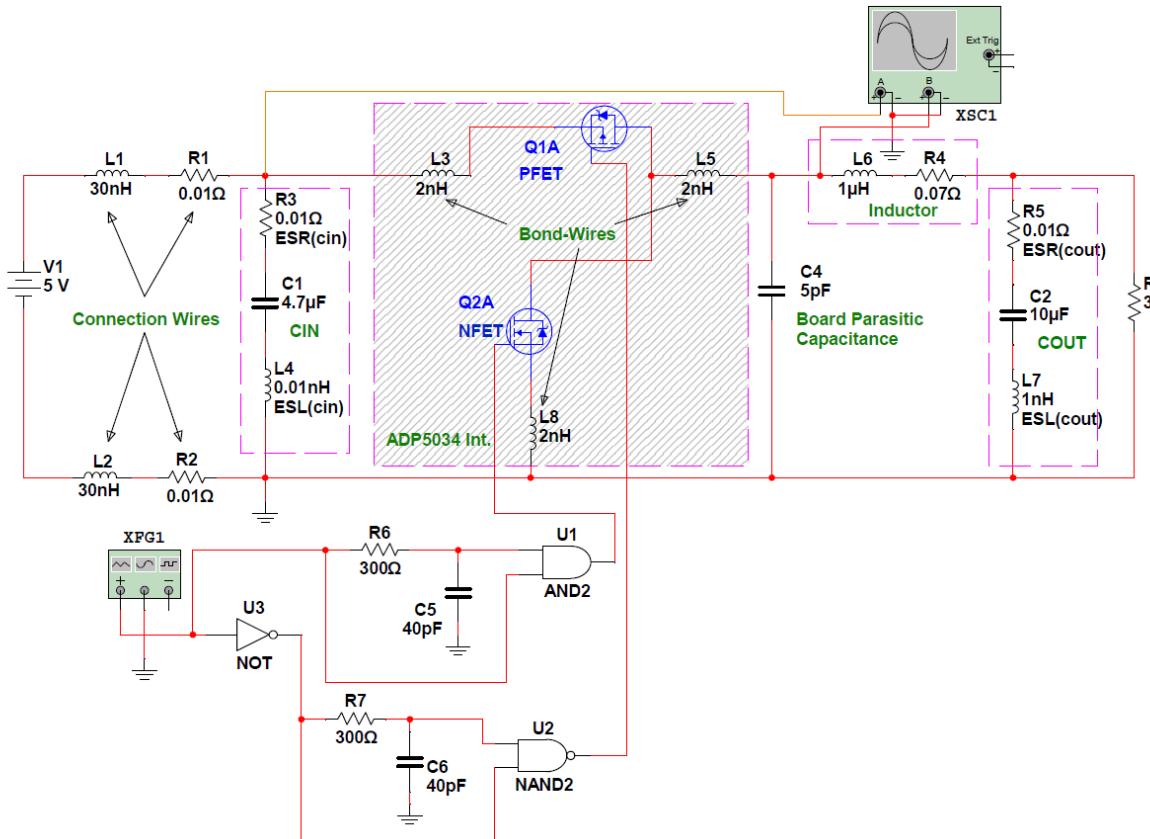
CIN ESL = 0nH (Ideal case)
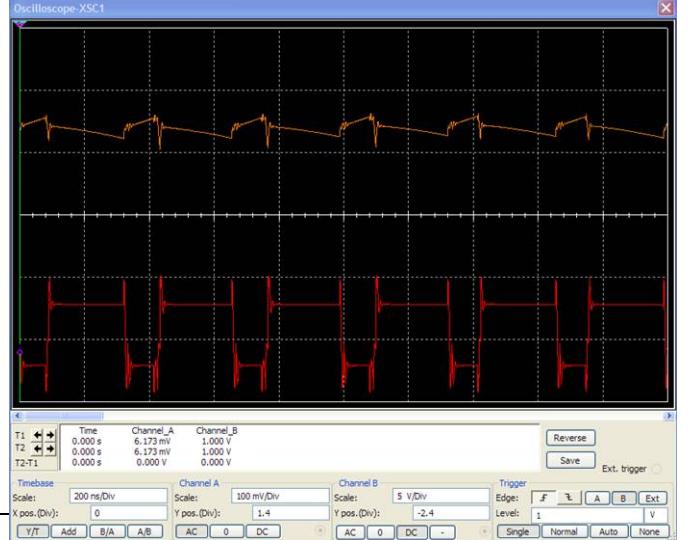
Fast di/dt transitions excite the circuit resonance which create the high frequency ringing. This high frequency noise affects performance of RF components

Reducing Switcher Noise

- **Reducing high frequency noise with small LC filters**
  - LDOs cannot effectively filter high frequency switching noise above the 0dB frequency of the LDO
    - LDO essentially becomes a RC filter formed by the output capacitance and the resistance determined by V_{DS}/Load Current
  - Filtering the input to the LDO with a small ferrite bead can improve high frequency by more than 20dB
  - Careful at parasitic capacitance of ferrite beads or inductors (SRF)
- **Careful on how to close the LDO loop**
  - Post filter can crate additional phase lag and make LDO unstable
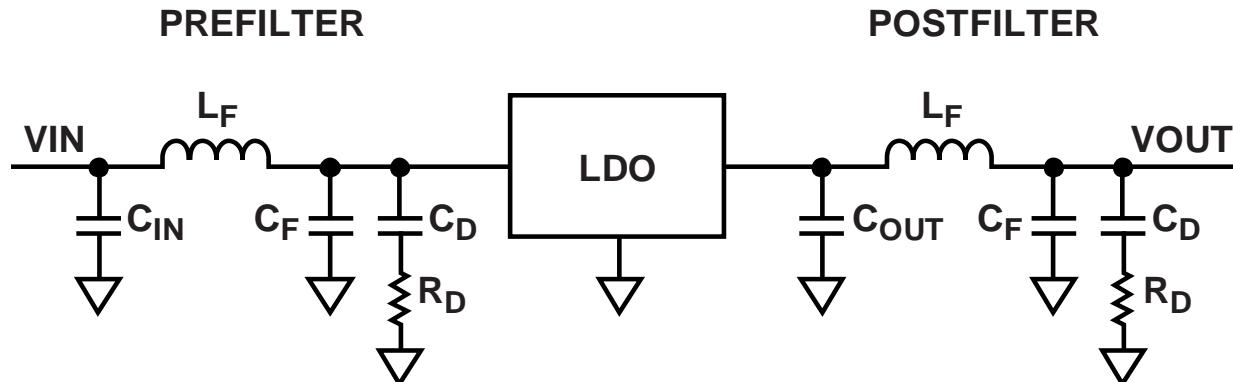
Powering 2 ADCs AVDD and DVDD rails directly from a switching regulator

- **Layout, component placement and selection is very important**
- **Dual Feedback loop AC and DC paths**
 - **Implemented for 2x AD9467/62 (16bit/ 250Msps ADC)**
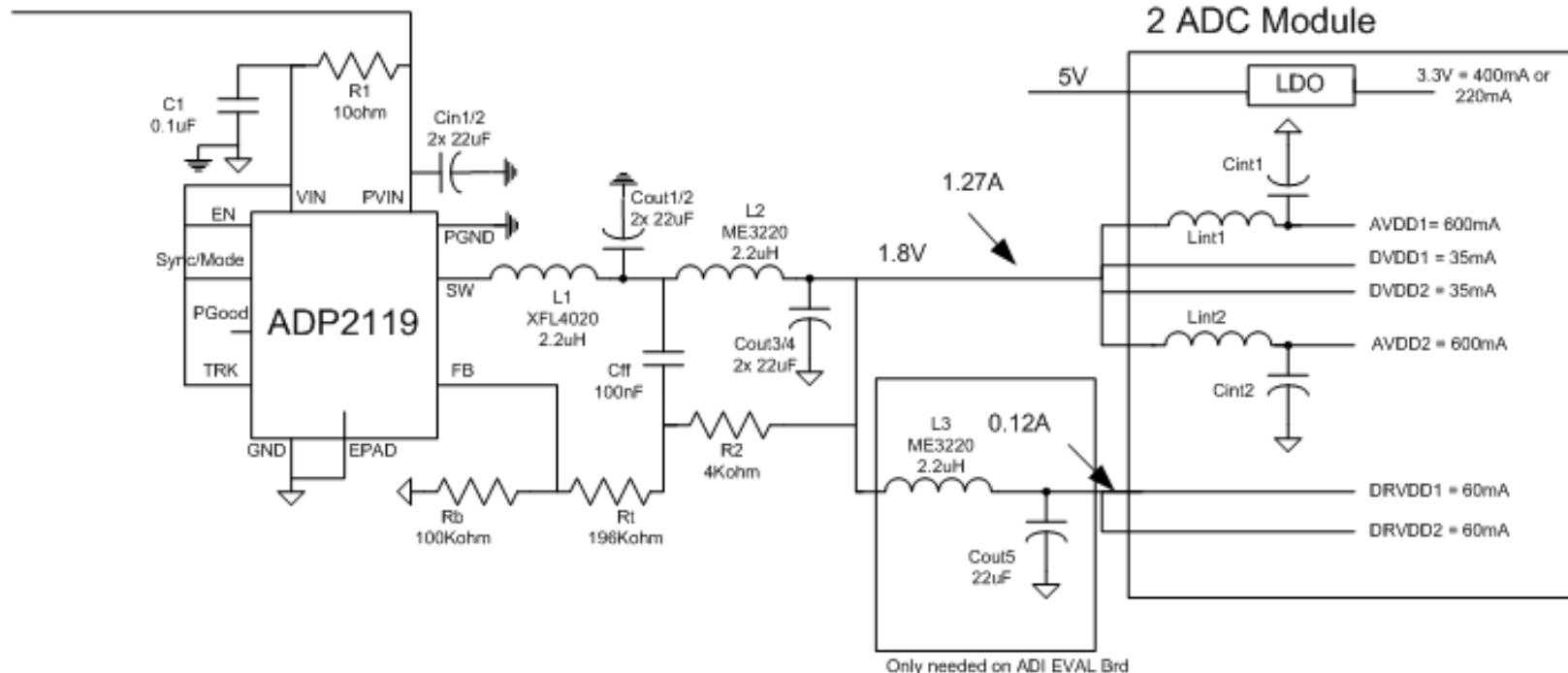
ADP2119 low noise design

- ◆ **Can achieve 147uVrms**
- ◆ **This is 5-10x worse than a decent LDO**
- ◆ **but easily 5-10x better than a standard switching regulator design**
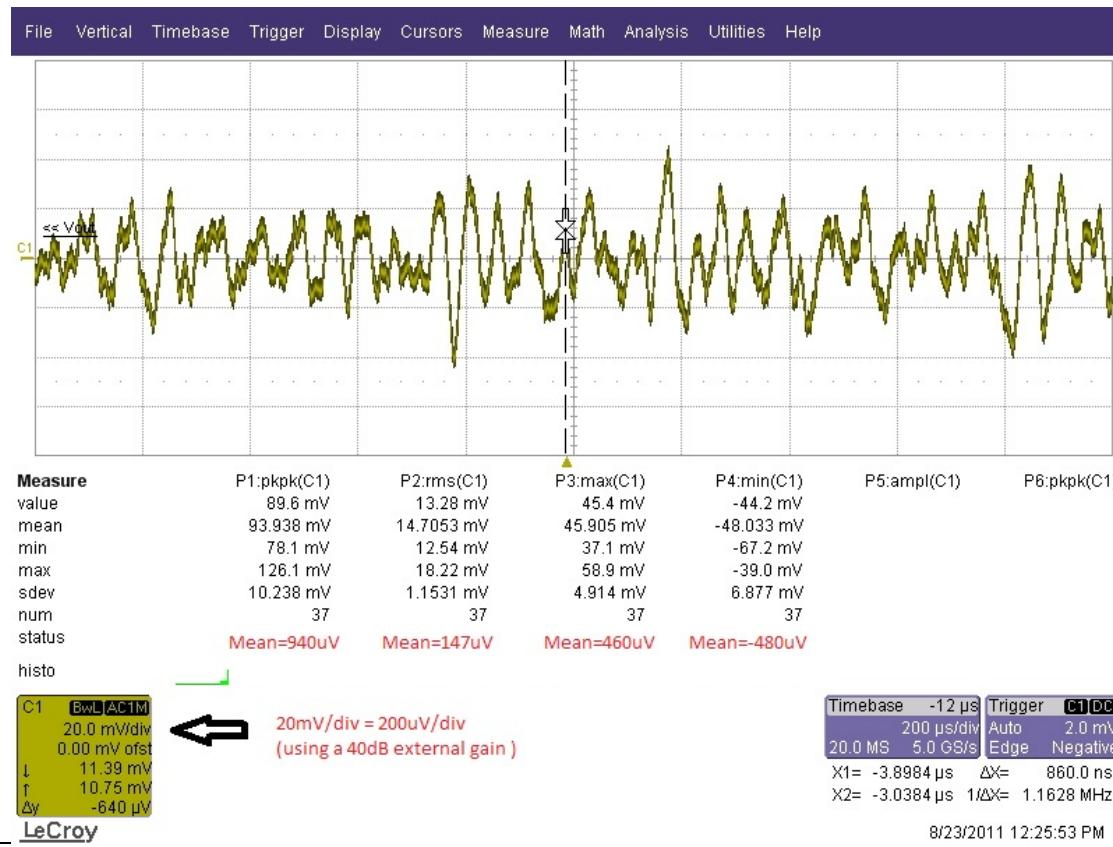
Performance comparison between LDO and ADP2119 results at -1dBm and -30dBm

SFDR
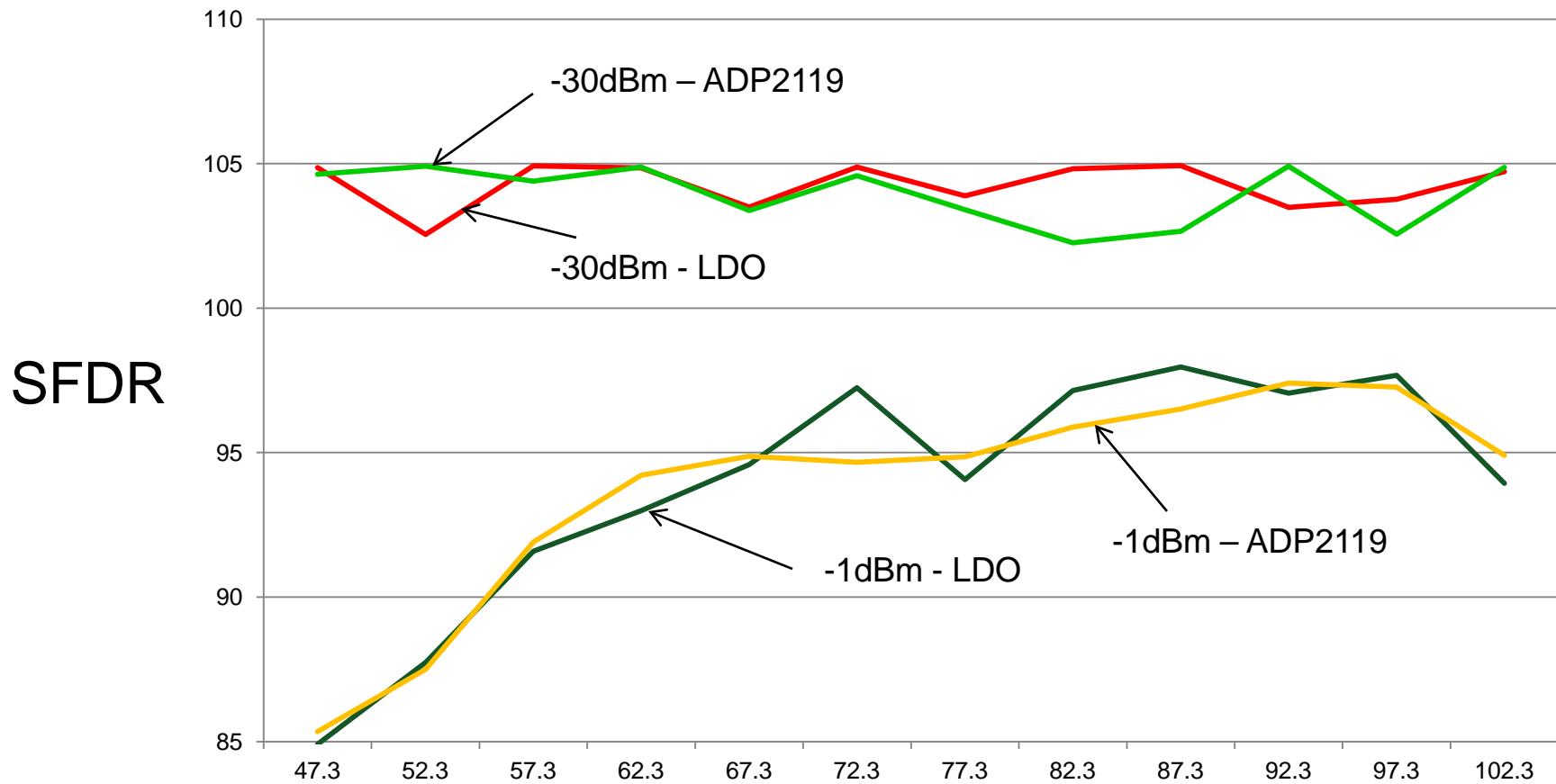
No performance degradation using the proposed ADP2119 design

43
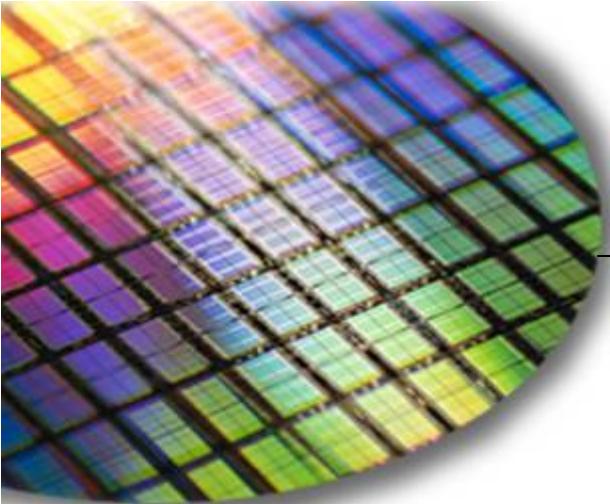
How to design a low noise switching regulator in 5 minutes

ADIsimPower VOLTAGE REGULATOR DESIGN TOOL

ANALOG DEVICES

What is ADIsimPower?   (sim: simple)

◆ **Smart Web based IC selector and performance ranking based on user operating conditions, with downloadable design tools**
  - **Web interface provides relative performance between topology and parts**
  - **Design tool downloadable for optimization by engineer**

◆ **Includes integrated "solution" selection guide**

◆ **Produces a Schematic and BOM optimized for your application**
  - **Downloadable for engineering use and documentation**

◆ **Requires no registration and no login**

◆ **Architected, designed, and used by PMP Apps Engineers**

It's an Optimization Tool

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Where do I find ADIsimPower

- ◆ **Start with the web based selector giude**
  - ◆ **www.analog.com/ADIsimPower**

Welcome to ADIsimPower™   The fastest and most accurate DC-DC Power Management design tool!

ADIsimPower is a collection of downloadable Excel spreadsheets that produce complete power designs optimized to your design goals. Get a schematic, bill of materials, and performance data customized to your specific needs in minutes. Select your favorite inductors, fets, diodes and capacitors. You can even order an evaluation board to build and test your design. ADIsimPower can optimize designs for cost, area, efficiency, and parts count. The designs produced are so accurate our Power Application Engineers use them.

Enter your design criteria below to use the web-based selector guide to compare all ADI's solutions and choose the one best fitting your requirements. If you already know the IC you want to use, select the "Download" link to access the tools.

Please note: The spreadsheets are several Megabytes in size and may take some time to download depending on your connection speed. You will need to enable macros to run each spreadsheet. In a small number of cases, solutions may be known to exist but a tool is not available yet.

All fields are required.

Vinmin (V)	Vinmax (V)	Vout (V)	Iout (A)	Tmax (°C)
4.5	5.5	1.2	1.0	55
$1.00 \leq x \leq 75$	$1.00 \leq x \leq 75$	$-85 \leq x \leq 90$	$0.01 \leq x \leq 60$	$-40 \leq x \leq 125$

Find Solutions	Use Dual Channel Device	Clear Fields

- ◆ **Many other ways to get there from Power Product pages**

Enter values and click on **ADIsimPower** to find power management solutions.

Available System Voltage		Operating Voltage Rail		Load Current	
Vin (min) ___ V	Vin (max) ___ V	Vout ___ V		Iout ___ A	

ADIsimPower VOLTAGE REGULATOR DESIGN TOOL

ADIsimPower Selector Results

◆ **Compare results based on solutions level performance**

ADIsimPower support multiple topologies

Tools by Parts

- **Linear Regulator**
  - **Supports all Linear Regulators**
  - **Also include parametric search**

- **Switching controllers**
  - **Buck: ADP182x, ADP187x, ADP1864, ADP185x**

- **Switcher Regulators**
  - **ADP21xx, ADP23xx, ADP232x, ADP237x, ADP238x, ADP3050, ADP2114_16, ADP505x**

- **Boost Switchers**
  - **Regulators: ADP161x**
  - **Controllers: ADP1621**

- **Buck/Boost**
  - **ADP2503_04**

Tools by Topology

- **Linear**

- **Buck**

- **Inverting Buck Boost**
  - Use a buck to create an inverting rail

- **Boost**

- **Cuk**
  - **Create an inverting rail**

- **Sepic**
  - **Vin greater or smaller than Vout**
  - **Example Vin = 9-15, Vout = 12V**

- **Sepic_Cuk**
  - **+/- rail**

- **Buck/Boost**
  - **i.e. 4 switch Buck boost**

ADI_LinearRegulators_Release.xls
ADI_SupervisoryTool_2010B.xls
AdiPowerDiscovery_Release.xls
ADP21xx_BuckDesigner_Release.xls
ADP161x_BoostDesigner_Release.xls
ADP161x_SEPIC_Cuk_Designer_Release.xls
ADP161x_SEPICDesigner_Release.xls
ADP182x_BuckDesigner_Release.xls
ADP187x_BuckDesigner_Release.xls
ADP230x_BuckBoostInvert_Release.xls
ADP230x_BuckDesigner_Release.xls
ADP232x_BuckDesigner_Release.xls
ADP237x_BuckDesigner_Release.xls
ADP238x_BuckDesigner_Release.xls
ADP1621_BoostDesigner_Release.xls
ADP1621_CukDesigner_Release.xls
ADP1621_SEPICDesigner_Release.xls
ADP1850-77_BuckDesigner_Release.xls
ADP1851_53_BuckDesigner_Release.xls
ADP1864_BuckDesigner_Release.xls
ADP2114_16_BuckDesigner_Release.xls
ADP2503_04_BuckBoostDesigner_Release.xls
ADP3050_BuckDesigner_Release.xls

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Tool use review: ADP238x Buck Designer

Tool use review: ADP238x Buck Designer

Set ripple target down to mV levels

Tool use review: ADP238x Buck Designer

Customize design by selecting parts from top to bottom · Enter Inputs

Item #	Des	MFG	Component Specs	Part Number	Pkg	Qty	Area (mm²)	Height (mm)	Cost*
1	IC	ADI	Switching Regulator	ADP2384ACPZN	24-Lead LFCSP	1	16.0	0.75	1.740
2	L1	Coilcraft	3.2uH, 6mΩ, 8.5Apk	SER1052-322MLB	11.2mm x 10.4mm x 5.2mm	1	116.0	5.2	0.910
3	Cin1	Taiyo Yuden	4.7uF, 16V, 9mΩ	EMK316 BJ475KL-T	1206	1	5.1	1.6	0.050
4	Cout1	Suncon	1800µF, 6.3V, 16mΩ	6ME1800WGL2	8mm	1	64.0	20	0.122
5	Cbst	Any	10% tolerance	100 nF, >20V	0805	1	2.5	0.5	0.005
6	Rf1	Any	1% tolerance	64.9 kOhms	0805	1	2.5	0.5	0.005
7	Rf2	Any	1% tolerance	16.2 kOhms	0805	1	2.5	0.5	0.005
8	Cc1	Any	10% tolerance	3.3 nF, >6V	0805	1	2.5	0.5	0.005
9	Cc2	Any	10% tolerance	68 pF, >6V	0805	1	2.5	0.5	0.005
10	Rc1	Any	1% tolerance	316 kOhms	0805	1	2.5	0.5	0.005
11	Css	Any	10% tolerance	56 nF, >6V	0805	1	2.5	0.5	0.005
12	Cvreg	Any	1uF, 10V, X5R	Generic	0603	1	1.3	0.6	0.005
13	Rt	Any	1% tolerance	215 kOhms	0805	1	2.5	0.5	0.005
14	Ren1			Short Out					
15	Cin2			Not Used					
16	Cout2			Not Used					
17	Ren2			Not Used					
18	Ren3			Not Used					
19	Rt1			Not Used					
20	Rt2			Not Used					
21	Rpg			Not Used					
22	J1			Not Used					
23	Eval Board	ADI		ADP2384-PRD1379		1			
* Cost is for distributer 1k or reel pricing. It is provided for comparison purposes only					**Totals**	**14**	**222.4**	**20**	**2.867**

Efficiency

Linear/Log Graph

Efficiency (y-axis): 0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1
Iout (A) (x-axis): 0, 0.5, 1, 1.5, 2, 2.5, 3

Legend: Vinmax, Vinmin

Provided Specifications

Vinmin	12 V
Vinmax	12 V
Vout	3 V
Iout	3 A
Ambient Temp	55 °C
Design Optimized for	Most Efficient

Advanced Target Settings

		Actual	Units
Height (max)	100	20	mm
ALL MLCC Capacitors	N		
All surface mount	N		
Shielded inductor	N		
Frequency Sync	N		
Frequency Select	Auto Frequency		
Switching Frequency	300		kHz

Product Features

Low Side FET	Don't care	Internal
SS_time	Auto Set	11.29	msec
Power Good	Not Used	
Tracking Configuration	No Tracking	

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Designing with ADIsimPower

- **Design performance summary including schematic and Customizable BOM**

ADP505x something new from ADI

- **Multichannel switching regulators (aka Packwood)**
- **Ideal for low noise system level designs**
  - **4.5V to 15V input**
  - **2x4A + 2x1.2A + LDO**
  - **Clock management and many additional features in one small package**

Generic	Number of Outputs	Vin (V)	Vout (V)	Max Output Current	Switching Freq Range	I2C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List
ADP5050	2x 2.5A Bucks	4.5V to 15V	0.8V to 0.85*VIN	2.5A (4A Max)	250kHz to 1.4MHz	Yes	-	-	-	48-lead LFCSP	$4.39
	2x 1.2A Bucks		0.8V to 0.85*VIN	1.2A Max							
	1x 200mA LDO	1.7V to 5.5V	0.5V to 4.75V	200mA Max	-						
ADP5051	2x 2.5A Bucks	4.5V to 15V	0.8V to 0.85*VIN	2.5A (4A Max)	250kHz to 1.4MHz	Yes	0.5V (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	$4.59
	2x 1.2A Bucks		0.8V to 0.85*VIN	1.2A Max							
ADP5052	2x 2.5A Bucks	4.5V to 15V	0.8V to 0.85*VIN	2.5A (4A Max)	250kHz to 1.4MHz	-	-	-	-	48-lead LFCSP	$3.59
	2x 1.2A Bucks		0.8V to 0.85*VIN	1.2A Max							
	1x 200mA LDO	1.7V to 5.5V	0.5V to 4.75V	200mA Max	-						
ADP5053	2x 2.5A Bucks	4.5V to 15V	0.8V to 0.85*VIN	2.5A (4A Max)	250kHz to 1.4MHz	-	0.5V (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	$3.79
	2x 1.2A Bucks		0.8V to 0.85*VIN	1.2A Max							

Fixed and Adjustable Output Voltages

Wide Range of Switching Frequency Operation (250 kHz to 1.4 MHz)

Resistor Programmable Current Limit on Buck 1 and Buck 2

Simple Power Supply Sequencing

Frequency Synchronization Input or Output

LDO or POR/WDI Options

ANALOG DEVICES

# ADP5050 – 4 Bucks + LDO + I2C Interface in LFCSP
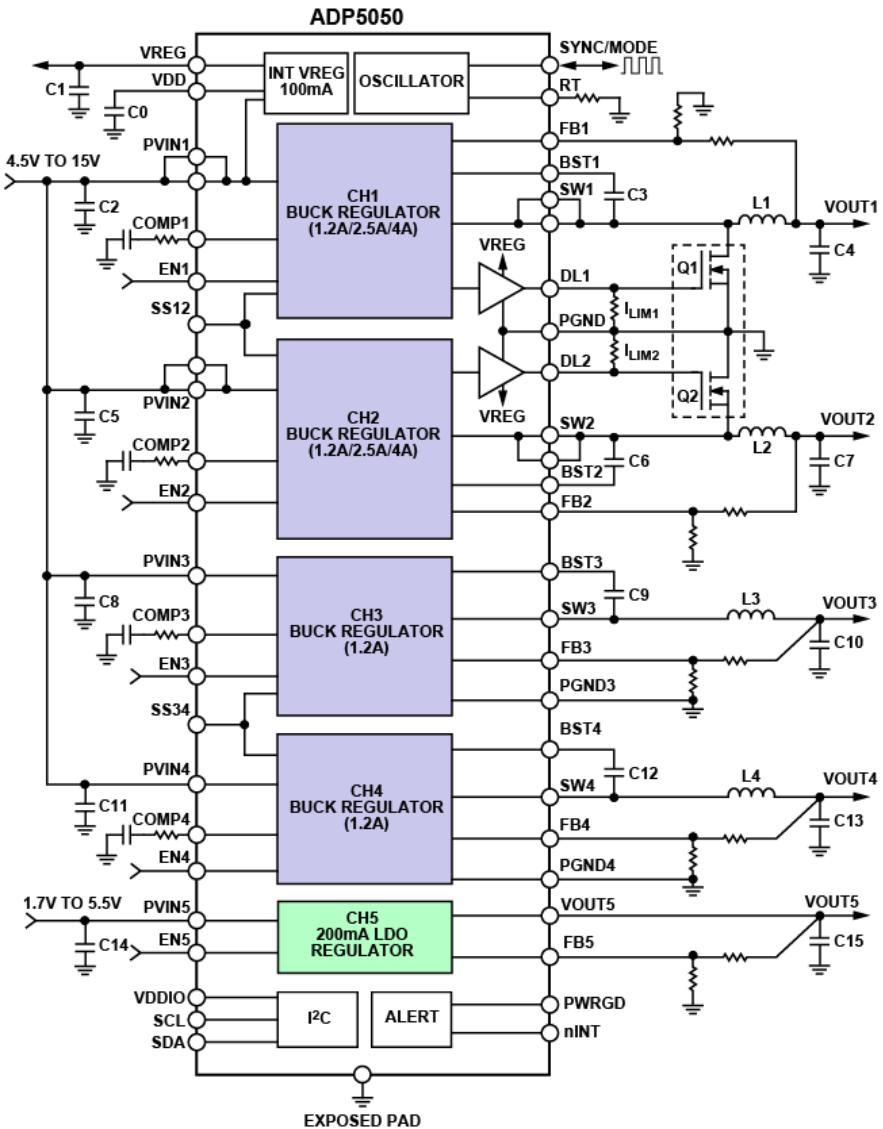
Key Features

- **CH1: Programmable 1.2A/2.5A/4A sync buck regulator with low-side FET driver**
- **CH2: Programmable 1.2A/2.5A/4A sync buck regulator with low-side FET driver**
- **CH3: 1.2A Buck Regulator**
- **CH4: 1.2A Buck Regulator**
- **Parallel CH1/CH2 to deliver up to 8A single output**
- **CH5: 200mA LDO**
- **Key Features**
  - *Wide Input Range: 4.5V to 15V*
  - *Adjustable/Fixed Output Voltage - via Factory or I2C*
  - *Pseudo-DVS: Dynamic Voltage Scaling*
  - *I2C interface with Interrupt Supportive on Fault Condition*
  - *250kHz~1.4MHz Adjustable Switching Frequency*
  - *Precision Enable on Accurate 0.8V Threshold*
  - *Programmable Current Limit*
  - *Phase-Shift (90˚, 180˚, 270˚) Programmable*
  - *FPWM/PSM Mode Selection per channel*
  - *Active Output Discharge Switch per channel*
  - *PWRGD Flag on Selective Channels*
  - *Frequency Synchronization Input or Output*
  - *Hiccup or Latch-off for Output-Short Protection*
  - *Low Input Voltage Detection*
  - *Overheat Detection on Junction Temperature*
  - *UVLO, OCP, OVP, TSD*
- **48 Lead 7mmx7mm LFCSP Package**
- **1k List Price $4.39**
- **Sampling Now**

Putting it all together
Powering the AD9368 a Radio on Chip Design
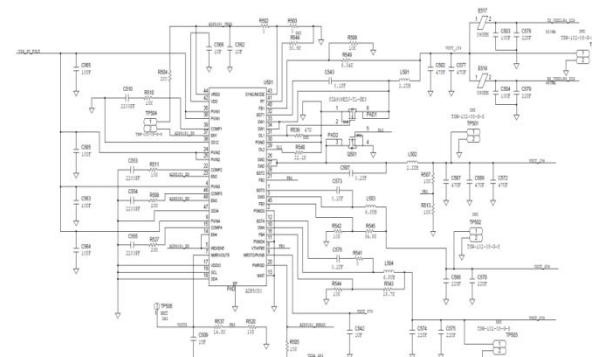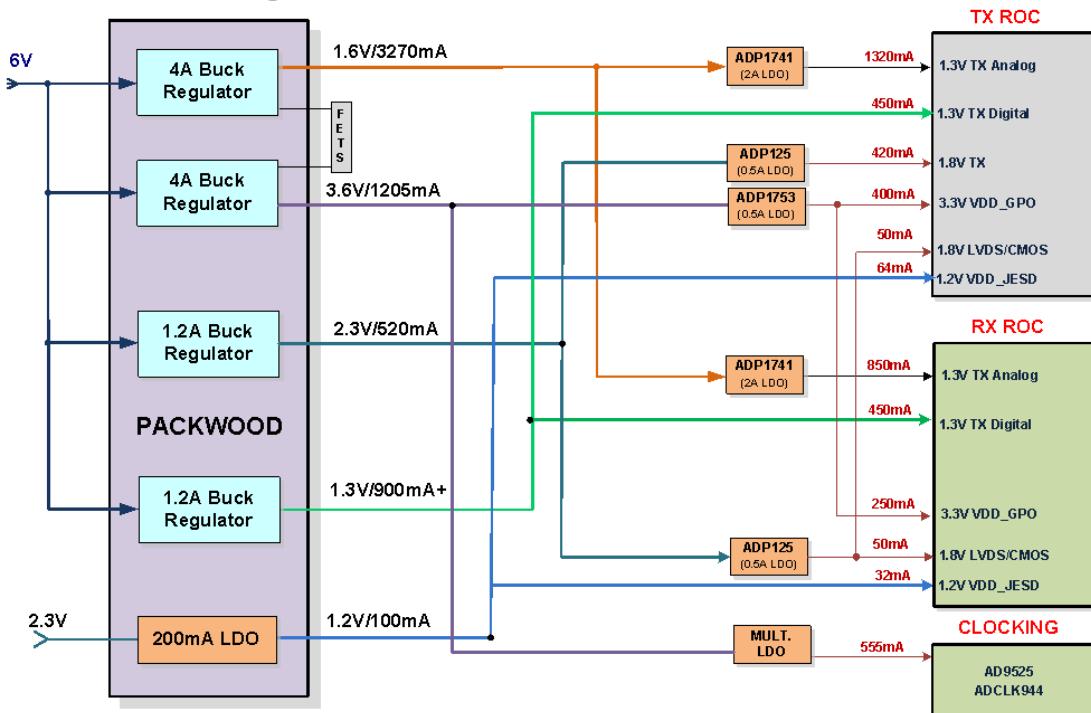
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- **Existing Arrow Customers: 800 777 2776**
- **New Customers: 800 833 3557**
  www.arrownac.com/powermanagement

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